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13. ABSTRACT *(Maximum 200 words)*

We summarize our second quarter progress and discuss third quarter plans for the development of an edge emitter based vacuum triode with performance goals of 10μA/μm emission current density at less than 250V and which can be modulated at 1 GHz for 1 hour. Design and layout of the emitter test mask was completed and fabrication of two process runs of edge emitter diodes were completed. These diode emitters utilize a comb emitter design where high resistivity TaN thin films act as current limiters to prevent edge burnout. Testing of these devices will start during the third quarter. Initial design work on the edge emitter triode was started and is described. Extensive finite element modeling (FEM) and analysis to aid in the triode design took place and is described. Significant process development also took place. Experimental studies of dielectrics such as sputtered SiO_2, Si_3N_4 and PECVD SiO_2 and Si_3N_4 were carried out to understand their leakage characteristics and, thus, understand their impact on emitter performance. A description of our vacuum test station is also given.

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Quarterly Technical Report

RF Vacuum Microelectronics

1/01/92 - 3/31/92

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10701 Lyndale Avenue South
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RF Vacuum Microelectronics
Quarterly Technical Report

I. Background

The objective of the RF Vacuum Microeelectronics Program is to establish the technology base for the fabrication of practical, high performance gated vacuum emitters and to develop a new class of RF amplifiers based on these vacuum microelectronic emitters. Our technical approach is to utilize thin film technology and surface micromachining techniques to demonstrate an edge emitter based vacuum triode with emission current density of 10 μA/μm at less than 250V which can be modulated at 1 GHz continuously for 1 hour. Figure 1 shows a schematic cross section of the type of our thin film edge emitter approach. Based on our experience with fabricating and testing edge emitter devices, our efforts on this program will be focussed on developing a highly stable, uniform and reliable current emission from the edge. We intend to achieve these qualities by

- use of thin film (200Å) edge emitters with small uniform radius of curvature
- use of refractory metal emitter structure to prevent electromigration and burnout
- use of comb emitter structures to prevent premature emitter burnout during edge formation
- use of current equalization series elements to set bias currents

This program to develop an edge emitter triode started on October 1, 1991. The baseline portion of the program is for 18 months with the above mentioned objectives as goals. Upon successful completion of this phase, an option phase for 12 months can be implemented by DARPA where the objective will be to achieve 10 GHz modulation with the edge emitter device.

II. Technical Progress During Quarter

Key Achievements (1-1-92 to 3-31-92)

- Developed thin film TaN resistor with 10^1-$10^6\Omega$/square resistivity.
- Completed field emitter test mask incorporating comb emitters and current equalization structures.
- Completed first run of diode field emitters.
- Began design of triode field emitter.
- Developed electromagnetic finite element model (FEM) of thin film edge emitter structure.
- Completed assembly of ultra-high vacuum test system with automated data acquisition.

III. Technical Progress

III-1 Field Emitter Development

We completed the two terminal device (field emitter diode) mask set. The mask set has a variety of devices that address the technical issues relating to the reliability of the emitter. Our previous work on field emitters based on thin film edges show that (i) the emitter burns-out during device operation, (ii) the edge does not emit uniformly, (iii) the emission current is not stable and (iv) the emission turn-on voltage is relatively high.

Our technical approach to addressing the issues include (i) use of thin film (≈200 Å) emitters, (ii) refractory metal comb structures to prevent burn-out, and (iii) current equalization with resistive elements to stabilize emission current. This also includes the use of layered emitter structures, heat treatment of the anode or the emitter with and without bias, and electropolishing of the emitters.

The mask set has devices that will test the above concepts. The device cross-section and layout is in Figure 1 while the process flow is shown in Figure 2. The mask has:

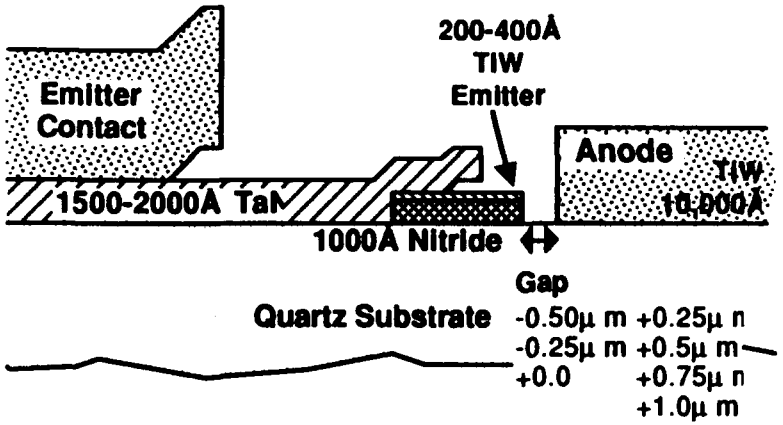
- Comb emitters with numbers (8-16) 1 μm and (4-8) 5 μm wide fingers
- Comb emitters with varying number of fingers, 1 μm and 5 μm fingers and current equalization resistors
- Continuous emitters with the same total width as the structures above.
- Continuous emitters with the same total width resistors

The gap between the anode and the emitter in all cases varied between 0.50 μm overlap and 1.0 μm gap in steps of 0.25 μm. This variation was done to allow for misalignment during lithography and over-etch or undercut of the emitter or anode layers.

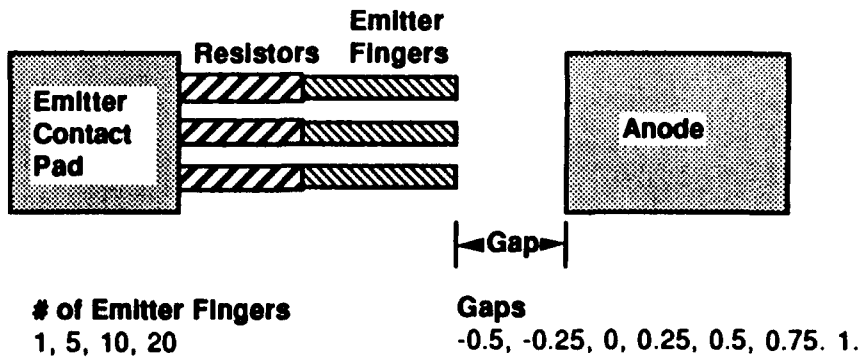
This set of devices will help us understand the burn-out mechanism and also determine if it can be controlled or abated by the comb structure or the current equalization resistors. The other devices on the mask include (i) heated field emitter diode, (ii) heated anode diode, (iii) field emitter diodes with ion probes, and (iv) multiple finger closely spaced devices to check on ion emission.

Figure 3 shows a composite plot of the five layers on the mask set. Each chip consists of nine die. Two dies are for process characterization while seven die consist of devices described above. Table 1 is a description of the devices and the purpose of the devices in the individual die.

We have completed the first process run of 12 wafers with this mask set. There are three splits of emitter thickness. (a) 200 Å TiW, (b) 300 Å TiW and (c) 400 Å TiW. Each split consists of three quartz wafers and a silicon wafer with 2.5 μm of silicon dioxide. Figure 4 is a photo of a completed device. The device shown has 5 μm comb emitters and series resistors. Parametric testing of these wafers has started and device testing will begin in early April. A second process run of wafers has begun.



Cross Section of Field Emitter Test Structure



Top View of Field Emitter Test Structure

- **Comb structure**
- **Thin-film emitter**
- **Thin-film resistor**

- **Emitter with and without combs**
- **Emitters with and without resistors**
- **Novel structures to determine electron trajectory**
- **Novel structures to determine positive ions or secondary electrons**

Figure 1. Device cross section and layout for typical emitter structure on mask set.

VME

TWO TERMINAL DEVICE
Process Flow

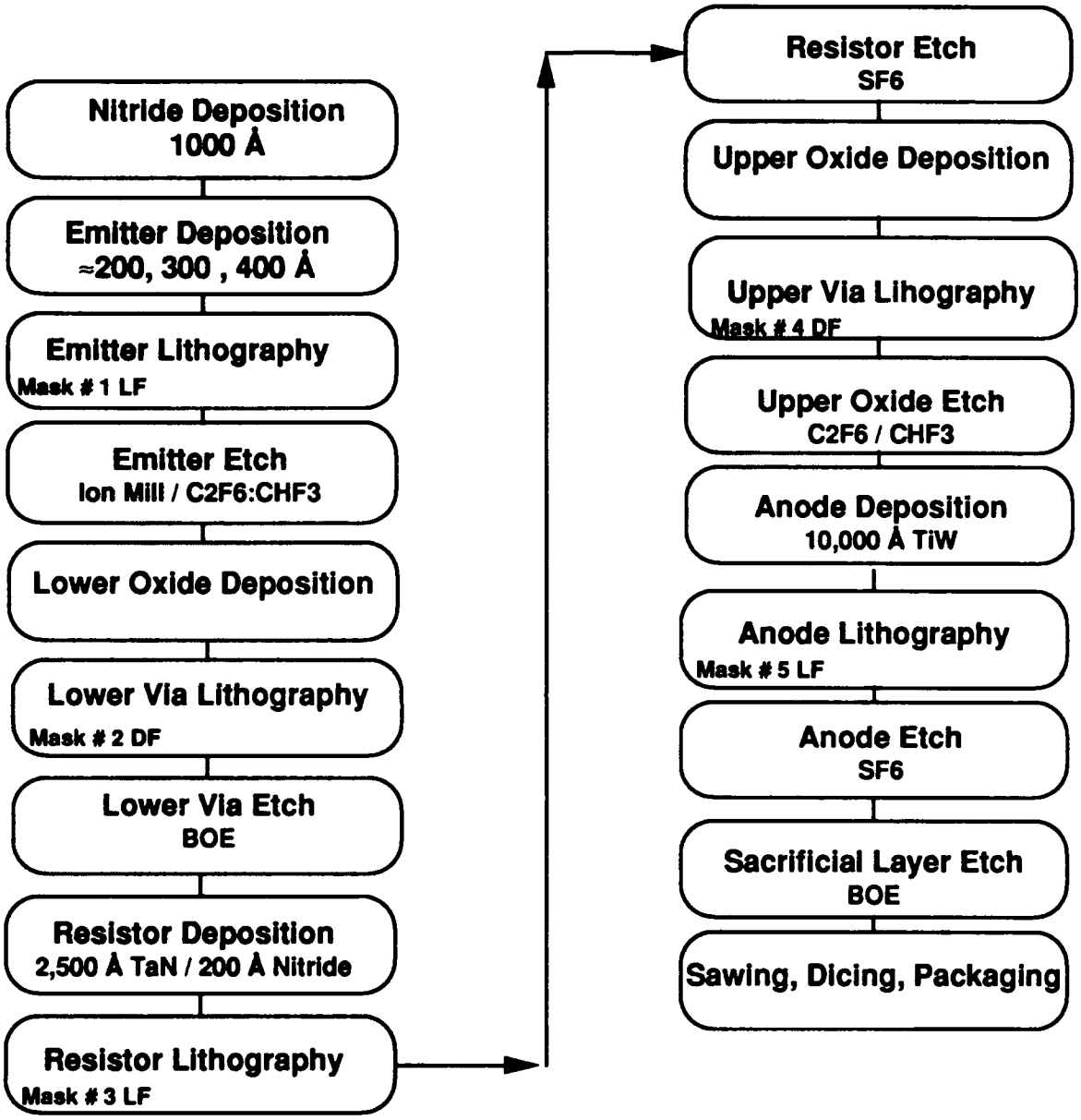


Figure 2. Process flow for two-terminal field emission device schematically shown in Figure 1.

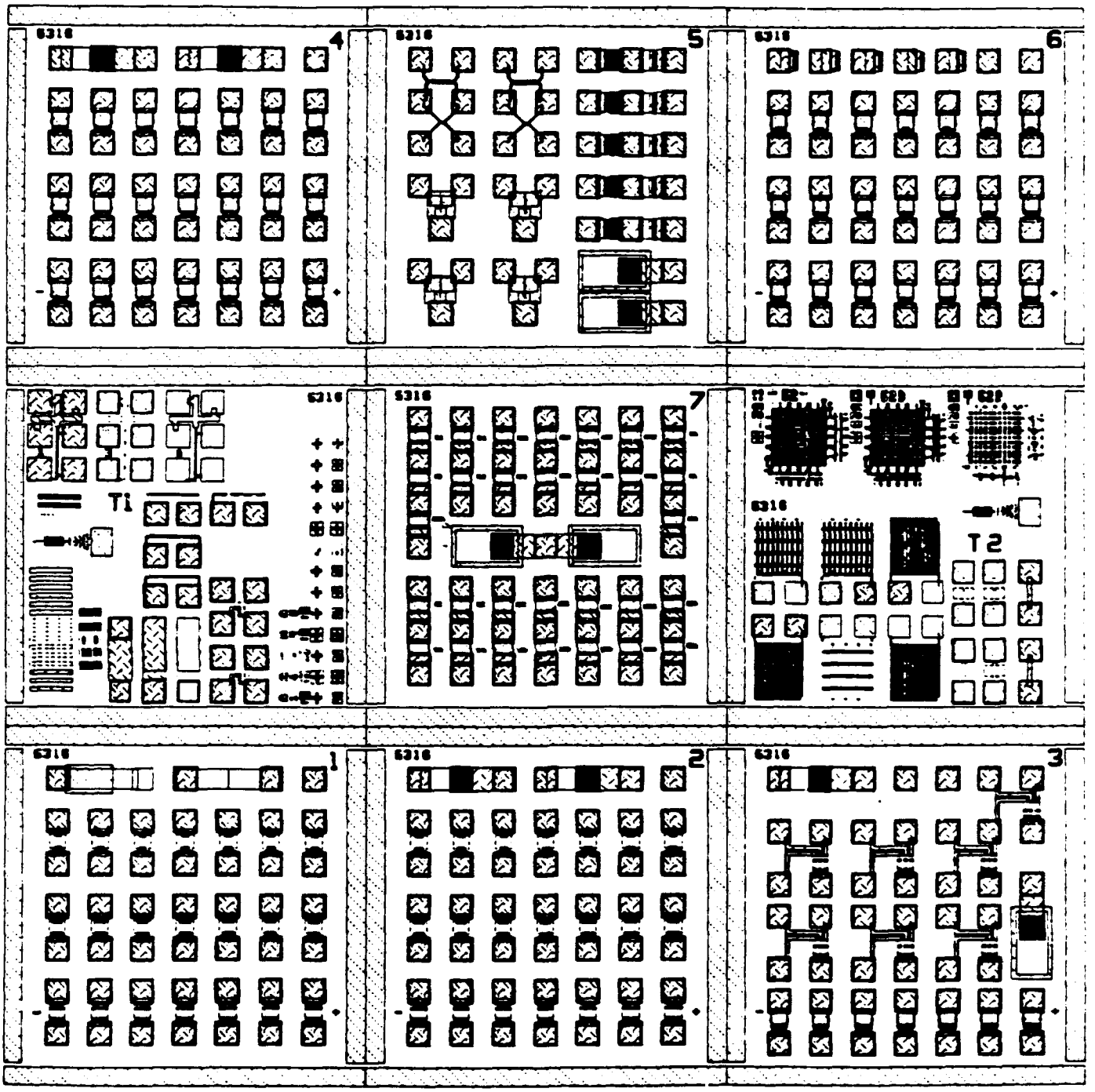
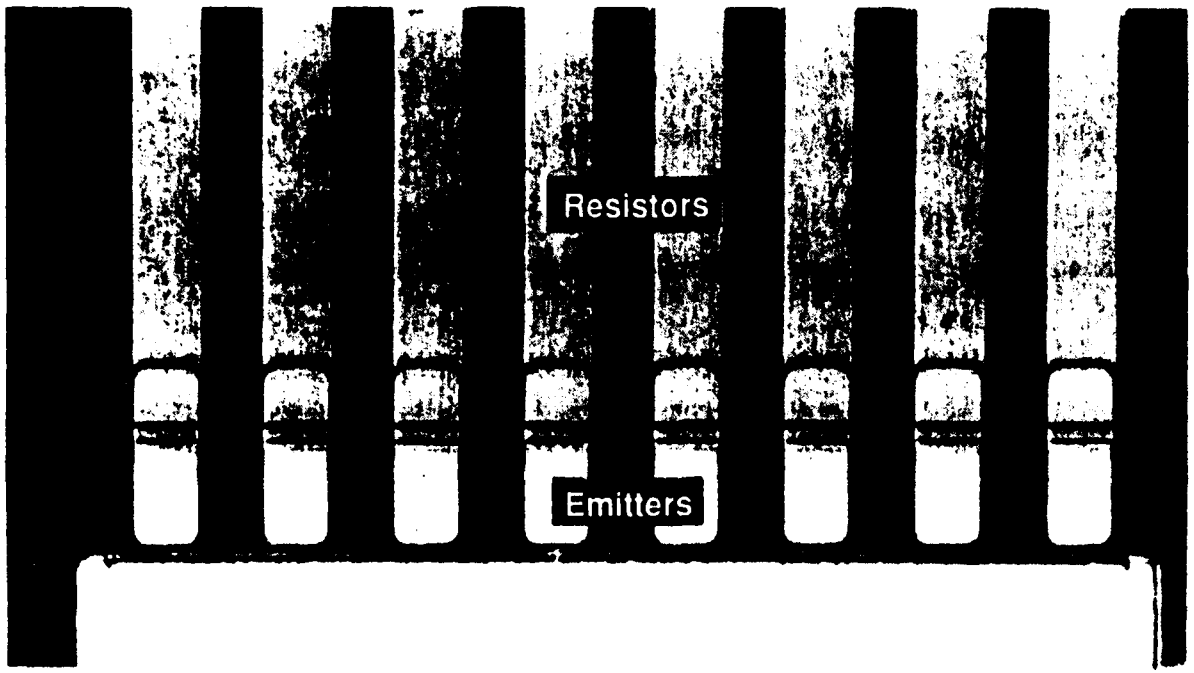


Figure 3. Layout of complete field emission diode reticle for mask 5316.



- **Completed process development**
- **Completed first run**
- **Testing to follow**

Figure 4. Photo of completed field emission test device. The TaN series resistors are 5 microns in width.

Table 1
Summary of Description of Individual Die

Die	Description	Purpose
1	5μm finger diodes with series resistors	Maximize current
2	1μm finger diodes with series resistor	Burnout diagnostics and current maximization
3	Emission uniformity test structures and 5 Mm finger diodes w/o resistors	Emission diagnostics
T1	Material measurement structures	Process characterization
7	Uniform and continuous edge emitter	Comparison with previous design
T2	Alignment marks, leakage test patterns	Alignment for lithography, process monitoring
4	Uniform and continuous edge emitter with series resistor	Comparison with previous design and burn-out diagnostics
5	Hot anode and emitter diodes, ion probes, ridge emitter	Emission diagnostics
6	1 μm finger diodes without resistors	Maximize current

III-2.1 Triode Design

The layout of the triode mask set has been initiated. Most of the triodes in this mask set have resistors in series with emitter fingers for current equalization. A typical structure is shown in Figure 5 has three fingers. The upper pad is connected to the anode, the lower pad to the emitters and the right hand pad to the upper and lower control electrodes. Figure 6 illustrates the active part of the device cross section. By etching both the resistor material and the emitter combs at the same time their connections are self-aligned enabling finger widths less than one-micron. Tantalum nitride thin films, developed on this program, offers flexibility in resistor values. The symmetric structure balances the electrostatic forces applied to the emitter by the upper and lower control electrodes and avoids excess force on the thin emitter film. Silicon nitride supports both the upper control electrode and the emitter for rigidity with low capacitance. For these test devices the size of the control electrodes will simplify processing. However, once high emission current density has been achieved, the control electrode lengths can be decreased for enhanced transconductance.

A preliminary list of the triode structures to be laid out for the triode mask set is given in Table 2.

Table 2

Preliminary Device List for Triode Mask Set

Device	Description	Total emitter widths (μm)
1	Multiple 1 micron wide emitters with series resistors	5, 10, 15
2	As above with emitter/resistor sandwich	5, 10, 15
3	Multiple 0.5 micron wide emitters with series resistors	5, 10, 15
4	Upper control electrode widths 3, 9, 15 and 19 microns	5, 10, 15
5	Multiple 1 micron emitters with multiple finger anode	5
6	Emitter array	

There will be additional test structures and the devices listed may be modified but the table describes most of the devices on the mask.

The design uses the masks described in Table 3 for maximum process flexibility and control of device characteristics.

Table 3

Triode Mask Levels

Mask Number	Description
1	Lower control electrode
2	Emitter course geometry
3	Emitter contact via
4	Resistor course geometry
5	Emitter and resistor comb etching mask
6	Dielectric cap definition for emitter edge
7	Upper sacrificial layer definition
8	Upper control electrode etching mask
9	Anode and pad contact window opening
10	Anode and pad definition
12	Optional upper control electrode support for short control electrodes

Figure 5. Field emission triode layout showing three 1-micron wide emitters with series resistors for current equalization.

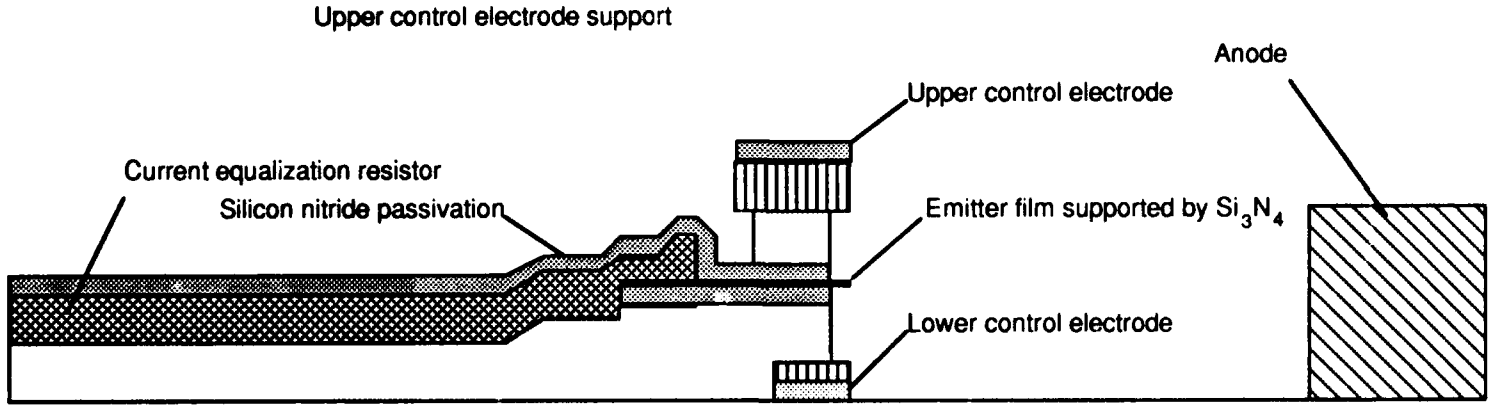


Figure 6. Schematic cross section of field emission triode showing arrangement of upper and lower control electrodes.

III-2.2 Triode Finite Element Modeling

Modeling Objective

The finite element modeling objective is to provide feedback regarding changes to the design of the triode structure and to determine their effect upon the electric field and field magnification factor at the emitter tip. The Fowler-Nordheim Law is used to relate field strength to the emitter current. Oxide thicknesses and the relative lateral spacings of the emitter and upper control electrode are the main effects that have been modeled to date. This modeling work fits well into the long term objective of developing an accurate tool for predicting and enhancing triode performance.

Model

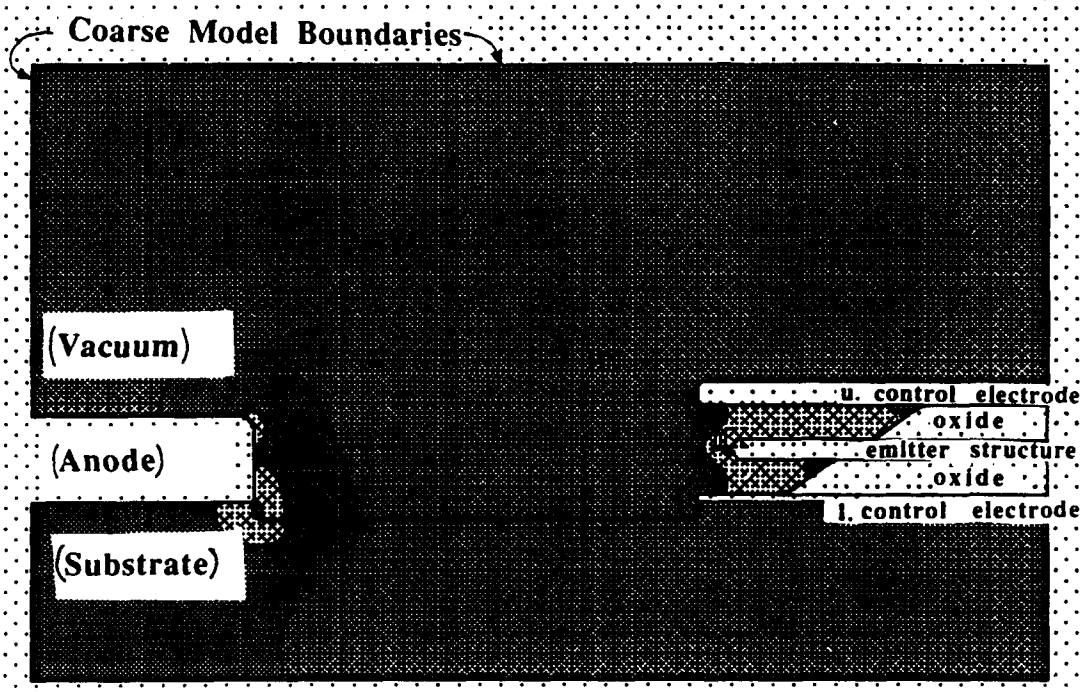
A two dimensional structure of the triode has been modeled using the ANSYS finite element program. Results are obtained through the numerical solution of Poisson's Equation. The model is fully parametized in order that geometrical variation studies may easily be performed. Both the actual triode structure as well as the surrounding vacuum and substrate material have been included; each material is assigned a dielectric constant and a permittivity. Voltage bias is applied to the upper and lower control electrodes (100 V) and to the anode (300 V). The emitter is placed at zero potential. As seen in figure 7, the anode continues out of the model off to the left. Likewise, the control electrodes and emitter continue out of the model off to the right. These structures can be considered to extend out in these directions infinitely. Under this assumption, Neumann boundary conditions have been applied to the left and right boundaries of the air surrounding the triode structure. This forces $dE/dx = 0$ and acts as a symmetry boundary condition. The upper and lower boundaries of the model cannot be treated this way however; they have been removed far enough from the region of interest that the field strength is significantly lower than the peak fields in and around the emitter tip. Along these edges, Dirichlet boundary conditions have been prescribed which constrain the boundary voltage to zero. Significant time has been devoted to boundary requirements and mesh density convergence studies; the most accurate and efficient values for each have been incorporated in the standard model.

Due to the extremely thin nature of the emitter, a significant E-field gradient is produced. In order to accurately represent this small region (the emitter is 250Å thick) in a model with boundaries as large as 10μm (a factor of 4000X larger), an extremely large amount of elements must be generated. In an effort to improve the model resolution and accuracy as well as to reduce the computational load, submodeling techniques has been employed. Also known as the cut-boundary conditions method, this approach uses the solution from a coarse model and applies the results to a separate, finely meshed region called the submodel. The submodel focuses in fairly closely on a small region around the emitter tip and has produced results of excellent resolution, detail, and accuracy (see figures 7 and 8).

Initial Results

Three studies have been initiated so far. One investigation sought to determine the dependence of emitter tip E-field vs. emitter position (the lateral position relative to the control electrodes). A similar study has evaluated the effect the lateral position of the upper control electrode has upon the emitter tip E-field. One final study looked at the dependence of the emitter tip E-field to the upper and lower control electrode spacing (by varying the oxide layer thickness). Since the sharpness of the emitter tip is unknown, a worst-case scenario has been used for the

Figure 7. Full F.E. Model View of E-Field Solution For a Vacuum Triode. (coarse model)

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APR   8 1992
17:43:14
POST1 STRESS
STEP=1
ITER=1
ESUM (AVG)
SMN =0.807056
SMX =882.492

ZV  =1
DIST=10.542
XF  =5.75
YF  =3.5
EDGE
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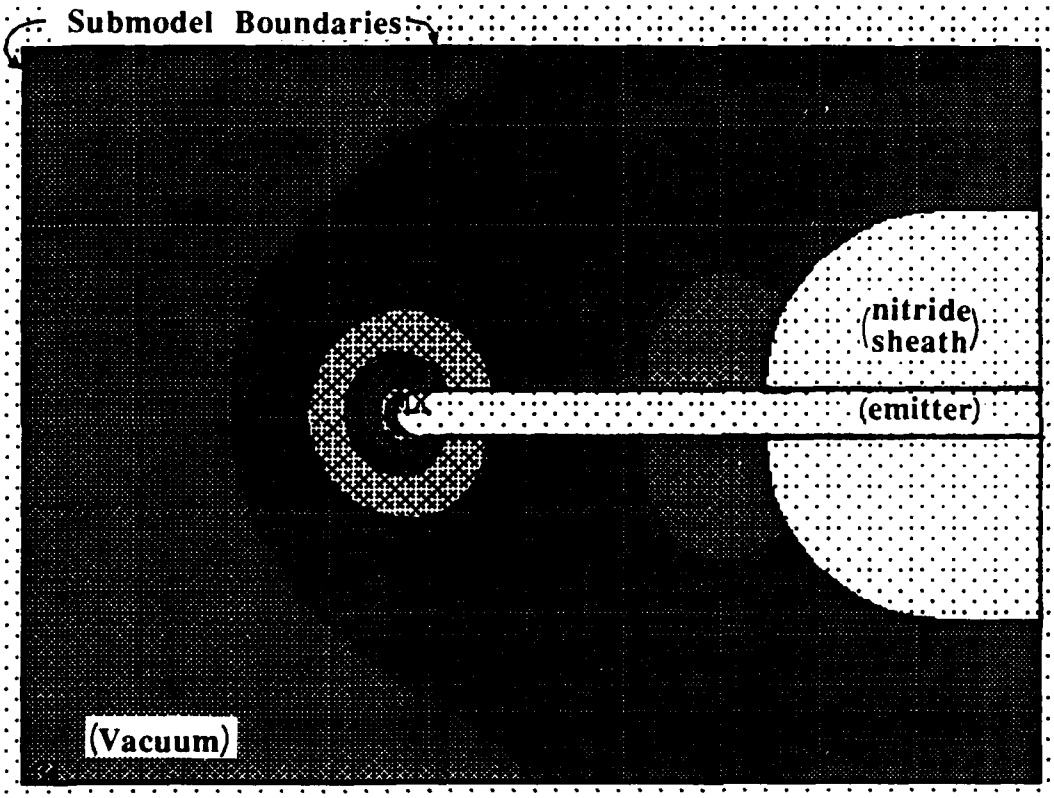
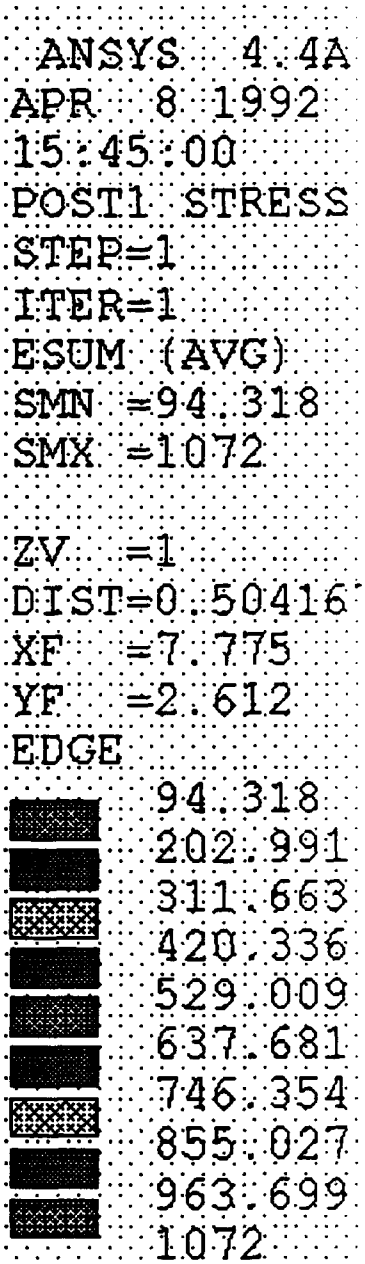
98.772
196.737
294.702
392.667
490.632
588.597
686.562
784.527
882.492

Vacuum Triode, Honeywell SSDC

Figure 8. Finite Element Submodel View of E-Field Solution in the Region of the Emitter Tip. (fine model)





Vacuum Triode, Honeywell SSDC

Figure 9a. Vacuum Triode, SSDC
Electric Field vs. Emitter/Control Electrode Positioning

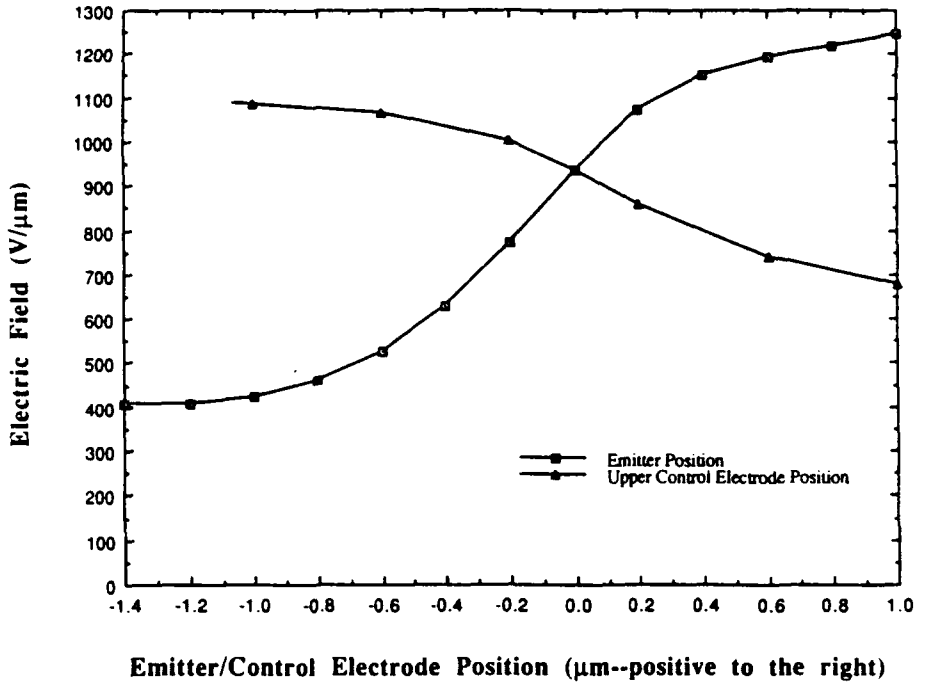
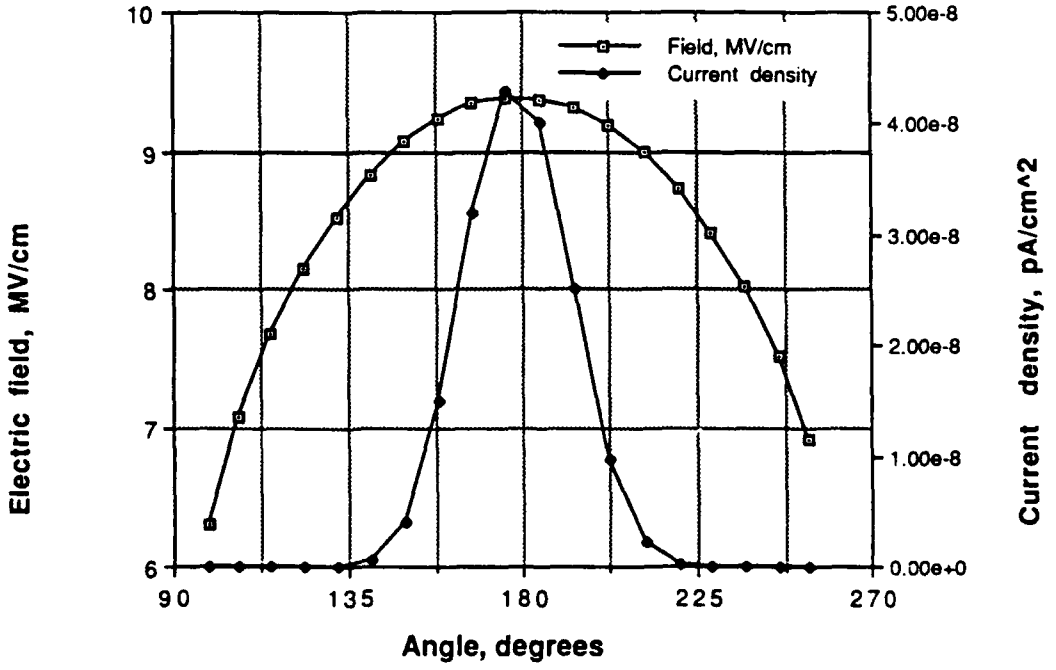


Figure 9b. Electric Field, Current Density
vs. Angular Position Around Emitter Tip



studies: the tip was given the smoothest edge possible, a fully rounded edge with a diameter equal to the film thickness (250Å).

Results show that the strongest electric field is produced when the emitter is retracted back in from the outer edges of the upper and lower control electrodes (see figure 9); a similar field enhancement is noticed when the upper control electrode is extended outwards from its aligned position. Perhaps the strongest field enhancement (up to 2X) is accomplished by decreasing the spacing between the emitter and control electrodes - an opposing effect will be a subsequent rise in leakage between the emitter and control electrodes; breakdown testing will be required to determine the optimum.

Attached is a full model plot of the coarse model , figure 7, (the emitter is barely visible due to its extremely thin dimension), a full model plot of the submodel, figure 8, a plot of the E-field at the emitter tip (figure 9a) as a function of upper control electrode position (0 = fully aligned with the emitter and lower control electrode, a positive value indicates that the electrode extends beyond the control electrodes to the left) and a polar plot of E-field and current density (figure 9b) for each node around the circumference of the emitter tip.

III-3 Test Set Up

The test set-up is shown in Figure 10. It consists of a small vacuum chamber with four 2.75 inch ports for manipulators. It is attached to a loading chamber of a PHI 430 MBE system that can be pumped below 5×10^{-9} torr. Six wafers can be loaded into a cassette and the wafers can be individually transferred by a magnetically coupled transfer rod to a bake-out chamber. The transfer stage is capable of receiving 3-inch wafers from the cassette and it can be heated to 700 °C. The wafers move from the transfer stage to the wafer testing stage which is capable of x, y in-plane motion of 0.75 inch and 360 ° rotation. The stage is also capable of 2 inch vertical travel.

Data acquisition is based on a 386-PC with LabTech notebook software. Two Keithley 237 power supplies and a Keithley 617 multi-meter are used for measurements.

We have written most of the test software and we are waiting for the microscope with 5-inch working distance and miscellaneous items for the probes before the system become operational. We expect the system to completely ready by the middle of April.

III-4 Dielectric Studies

A study of the dielectric films used in the VME structures was started to determine the quality of the films. There will be high electric fields present in the structures and the dielectric films must be of high quality with low leakage currents and high breakdown fields for proper device operation. The dielectric films used in the VME structures include both silicon nitride and silicon dioxide films deposited by sputter deposition and also by plasma enhanced chemical vapor deposition (PECVD).

Capacitor structures were fabricated using each of the dielectric films to test the leakage current and breakdown field strength. The capacitors consisted first of a patterned bottom metal electrode. This electrode was deposited over a silicon nitride film on a silicon wafer. The silicon nitride film was used to electrically isolate the capacitor structure from the silicon substrate. The dielectric film to be studied was then deposited over the metal electrode and then a top metal electrode was deposited and patterned over the film. Via holes were then cut to the electrodes and contact pad metals were deposited and patterned. The dielectric films used for this study were 1000Å thick films.

Vacuum Test Chamber

Vacuum Chamber

- All parts compatible with Perkin-Elmer PHI 430 MBE system
- Pressure ≤ 5 x 10^{-9} torr
- 2.75-in ports for micro-manipulators
- Wafer stage capable of X, Y travel ±0.75 in, Z travel 2-in and 360° rotation
- Transfer stage capable of receiving 3-in wafers and heating wafers to 700°C

Data Acquisition

- 386-based data acquisition system
- Keithley 237 power supplies
- Keithley 617 multimeter
- Triax cabling

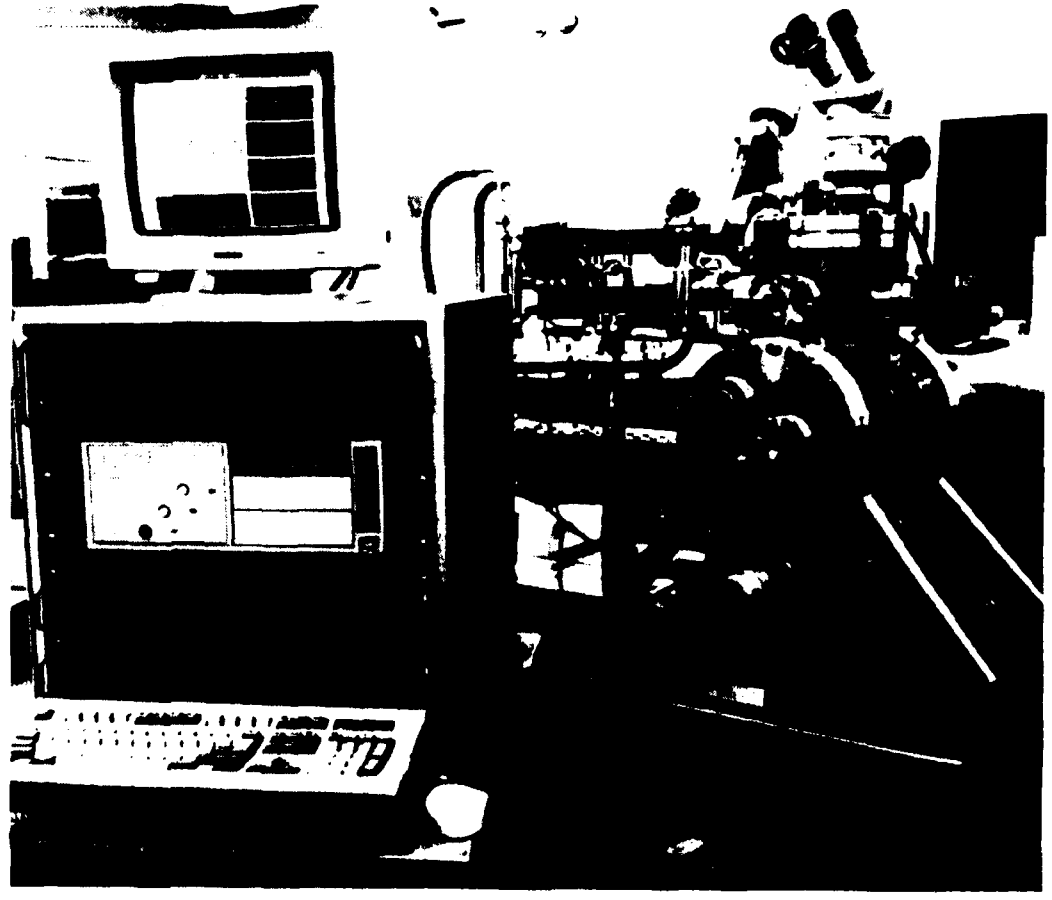


Figure 10. Test set-up at Honeywell SSDC for field emission device studies. We anticipate the system to be fully operational in mid-April 1992.

Current versus voltage measurements were made on the capacitor structures to measure the dielectric breakdown strength and current leakage of the films. The leakage current in the films was measured up to fields of 1.0e7 V/cm. The films were measured in the as-deposited state and after subsequent anneals in forming gas (N_2 and O_2) at temperatures of 250 °C, 300°C, 350°C and 500 °C. The following dielectric films were included in the study:

Sputtered Silicon Nitride - With High Bias

Sputtered Silicon Nitride - With Low Bias

Plasma-Enhanced Chemically Vapor Deposited (PECVD) Silicon Nitride

Sputtered Silicon Dioxide

PECVD Silicon Dioxide.

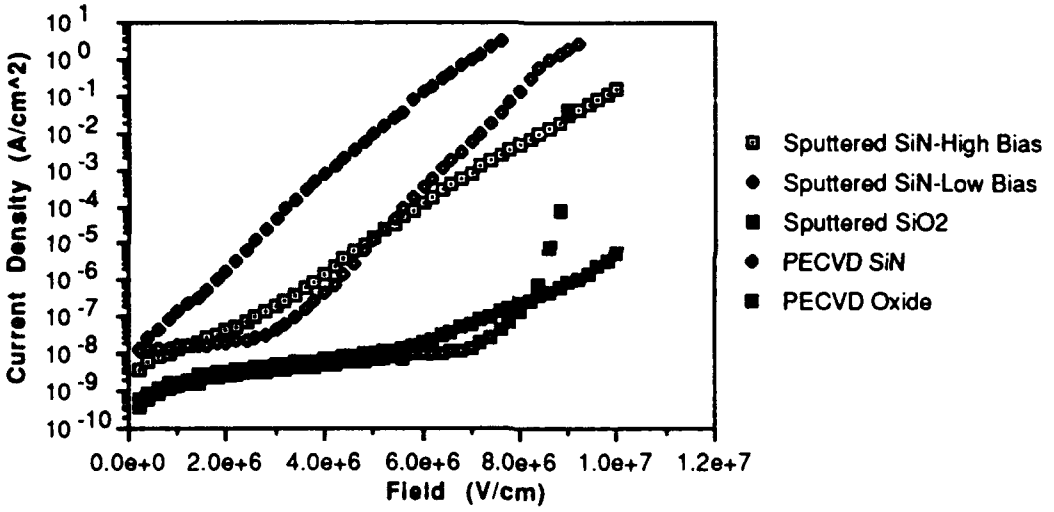


Figure 11. Composite Plot Of Current Density Versus Field For As-Deposited Dielectric Films

Figure 11 shows the measured current density versus electric field curves for each of the films in the as-deposited state with no annealing. The silicon nitride films show a relatively high leakage currents that increased with the applied field even though actual breakdown of the films does not occur until fields above 8.0×10^6 V/cm or higher. The high-bias sputtered silicon nitride and the PECVD oxide did not breakdown even at a field of 1.0×10^7 V/cm. Breakdown fields of $\geq 10^7$ V/cm are considered to be very good for silicon dioxide and silicon nitride. The oxide films though, showed very low levels of leakage current, below 10^{-7} A/cm^2 for fields below 8.0×10^6. These results indicate that the oxide films provide may provide better dielectric isolation between the active layers in the diode and triode structures.

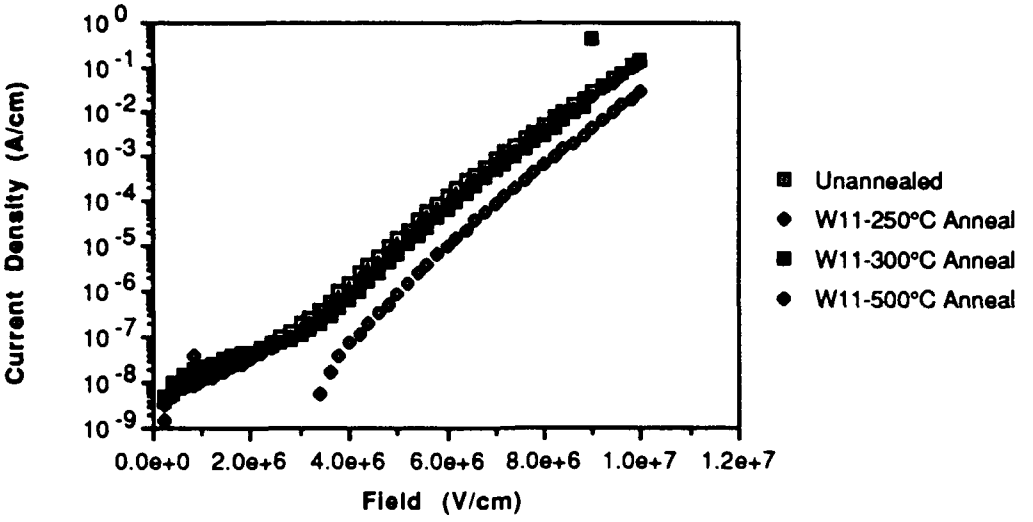


Figure 12. High-Bias Sputtered Silicon Nitride Film With Annealing

The dielectric films were annealed to see if there would be any improvement in the properties of the films. Figure 12 shows the results of annealing for the high-bias sputtered silicon nitride film. There was little change in the current-voltage characteristic with annealing up to the 500 °C anneal. After the 500 °C anneal the curve shifted so that the leakage current was smaller for the same field strength compared to before the annealing. The leakage current is still relatively high though and increases with the applied field.

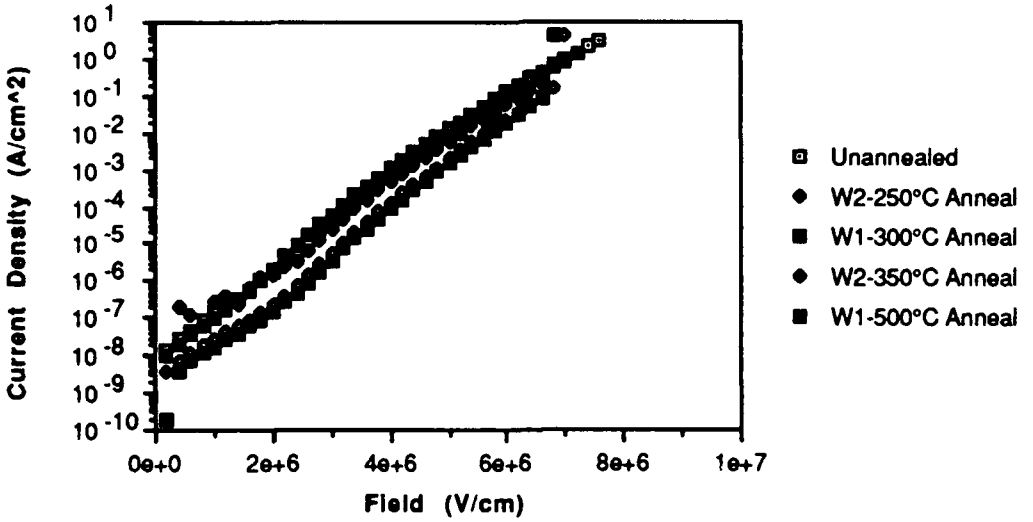


Figure 13. Low-Bias Sputtered Silicon Nitride Films With Annealing

Figure 13 shows the changes in current density versus field characteristics for the low-bias sputtered silicon nitride films. As in the case of the high-bias sputtered films, there was some improvement in the level of the leakage current with the 350 °C and 500 °C anneals, but there was also some lowering of the breakdown field strength of the films.

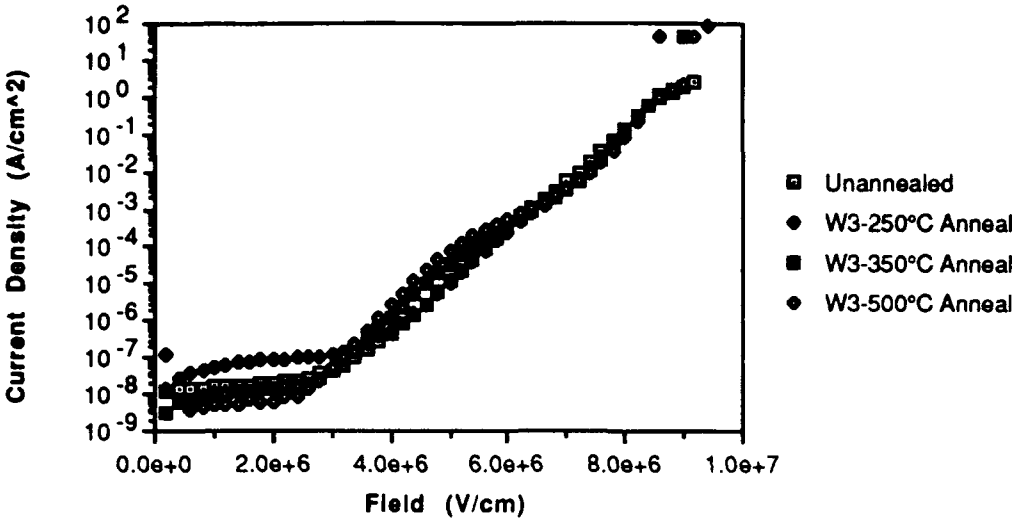


Figure 14. PECVD Silicon Nitride Films

The PECVD silicon nitride films showed no improvement in level of leakage current with annealing as shown by the characteristic curves shown in Figure 14. There was some curve shape changes but no lowering of the current density level or improvements in the breakdown field.

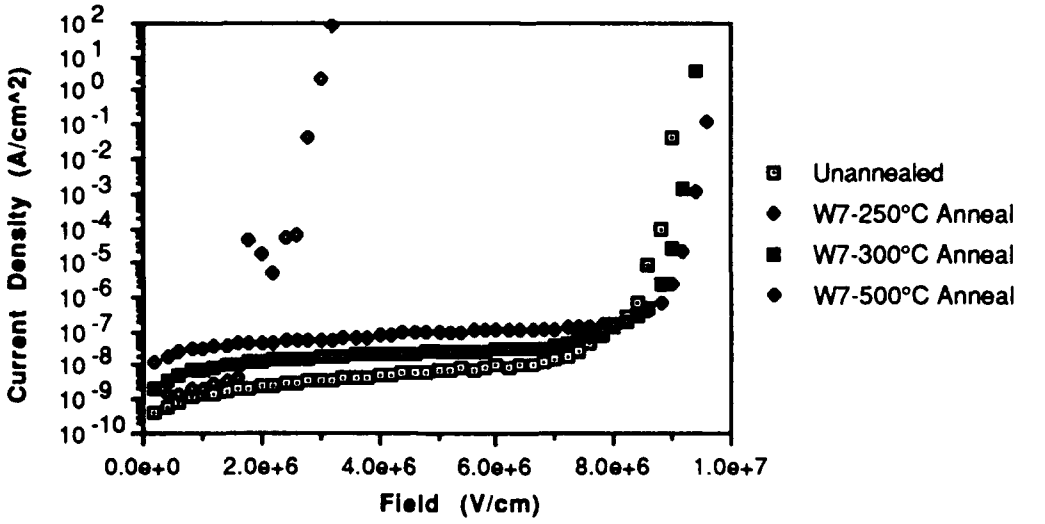


Figure 15. Bias Sputtered Silicon Dioxide Film With Annealing

Figure 15 shows the curves measured for a sputtered silicon dioxide film with annealing. The leakage current remains very low, $\leq 10^{-7}$ A/cm^2, to fields of up to 8.0 x 10^6 V/cm. The films breakdown between 9.0 x 10^6 and 1.0 x 10^7 V/cm which is good for these films. The current level increased with annealing and with the 500 °C anneal the film appeared to deteriorate and have a much lower breakdown field than the unannealed film.

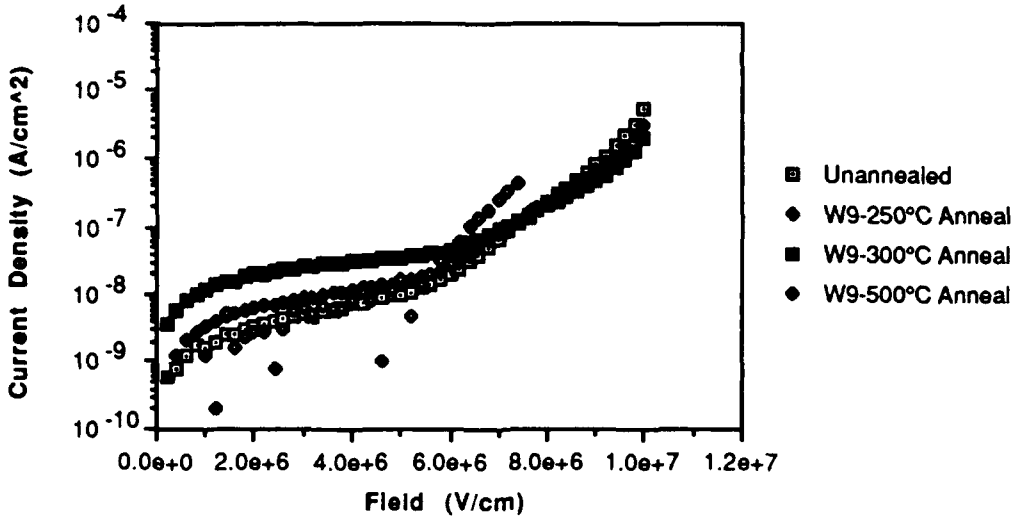


Figure 16. Plasma-Enhanced Chemically Vapor Deposited Silicon Oxide Film With Annealing.

Figure 16 shows the measured curves for a PECVD silicon dioxide film. This oxide film also shows low leakage current, $\leq 10^{-7}$ A/cm2, up to fields of 6.0 x 10^6 V/cm. Above this field, the leakage current rises but the breakdown field is still $\geq 10^7$ V/cm. Annealing results in some increase in the current level and after the 500 °C anneal the film measurement became erratic and the breakdown was lowered from that of the unannealed film.

Summary

Several of the silicon oxide and nitride dielectric films that will be used in the VME diode and triode structures have been evaluated for the quality of their dielectric properties. Leakage current and breakdown field strength were measured for each film. Annealing of the films was done to see if the dielectric properties of the films could be improved. The breakdown field strength of all the films was relatively high, at least 8.0 x 10^6 V/cm with some films $\geq$ 1.0 x 10^7 V/cm. The leakage current in the silicon nitride films was high and increased with the applied field. These films by themselves would probably not provide sufficient dielectric isolation between the active layers in the diode and triode. The oxide films, however, had much lower levels of leakage current and could provide the isolation needed in the structures. Annealing of the films provided some improvement in the silicon nitride films and some degradation of the oxide films. The highest anneal at 500 °C, lowered the breakdown field for the oxide films, but had minimal effect on the silicon nitride films.

In the diode and triode structures, the best dielectric isolation may be composite stacks of oxides and nitrides to maintain low leakage current and a high dielectric breakdown field between the active electrodes in the diode and triode structures.

IV Plans for Next Quarter

- Complete triode emitter design.
- Test diode edge emitters from first two process runs.
- Carry out emitter conditioning experiments to maximize current and eliminate burnout.
- Continue diode edge emitter fabrication with various emitter materials and processing conditions. Utilize test results for process iteration.
- Continue FEM analysis of triode structure. Evaluate triode designs to maximize field at emitter tip.
- Carry out atomic force microscopy of emitter materials to examine surface condition of the edge.
- Carry out edge smoothing experiments for the emitter edge using electropolishing, etc.